What is claimed is:

1. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a contact hole exposing a partial portion of the substrate by etching the inter-layer insulating layer;

forming a storage node contact buried into the contact hole such that the surface of the storage node contact is at the same plane level as the surface of the inter-layer insulating layer;

forming a storage node oxide layer on the inter-layer insulating layer;

forming a storage node hole exposing the storage node contact by etching the storage node oxide layer;

forming a supporting hole having a hollow form in a downward direction by partially removing an upper portion of the storage node contact exposed by the storage node hole; and

forming a storage node having a cylinder structure electrically connected to the storage node contact wherein a bottom portion of the storage node is disposed in the supporting hole supported by the supporting hole and the inter-layer insulation layer.

2. The method as recited in claim 1, wherein the storage node contact is a polysilicon plug and an upper portion of the polysilicon plug is recessed or removed at the step of forming

the supporting hole.

3. The method as recited in claim 2, wherein at the step of forming the supporting hole, the upper portion of the polysilicon plug is subjected to one of a dry etching process and a wet etching process.

4. The method as recited in claim 3, wherein the dry etching process is carried out by adopting an etch selectivity having a ratio of the polysilicon layer with respect to the storage node oxide layer of about 40 to 1.

5. The method as recited in claim 3, wherein the wet etching process uses one of a chemical solution mixed with NH_4OH at a mixing ratio which ranges from about 10 to about 1 and H_2O at a mixing ratio which ranges from about 1 to about 500, and a chemical solution mixed with HF at a mixing ratio which ranges from about 20 to about 1 and HNO_3 at a mixing ratio which ranges from about 1 to about 100.

6. The method as recited in claim 5, wherein the chemical solution is put into a dipping bath in which temperature is maintained in a range from about 4 °C to about 100 °C for about 5 seconds to about 3600 seconds.

7. The method as recited in claim 3, wherein, at the step of forming the supporting hole, a target thickness of the

polysilicon plug ranges from about 50 Å to about 5000 Å.

8. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a contact hole exposing a partial portion of the substrate by etching the inter-layer insulating layer;

forming a storage node contact buried into the contact hole such that the surface of the storage node contact is at the same plane level as the surface of the inter-layer insulating layer;

forming a storage node oxide layer constructed with a double layer of an upper layer and a lower layer, wherein an etch selectivity ratio of the upper layer formed on the inter-layer insulating layer is higher than that of the lower layer;

forming a storage node hole exposing the storage node contact by etching the storage node oxide layer;

widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer;

forming a supporting hole hollowed in a downward direction by removing a partial portion of an upper portion of the storage node contact exposed by the storage node hole whose width is widened; and

forming a storage node having a cylinder structure and being connected electrically to the storage node contact as a bottom region of the storage node within the storage node hole

is supported by the supporting hole and the under-cut region.

9. The method as recited in claim 8, wherein the step of widening the storage node hole and simultaneously forming the under-cut region at the lower layer of the storage node oxide layer uses a dip process using a wet chemical.

10. The method as recited in claim 8, wherein the storage node contact is a polysilicon plug, and an upper portion of the polysilicon plug is removed at the step of forming the supporting hole.

11. The method as recited in claim 10, wherein the upper portion of the polysilicon plug is etched using one of a dry type and a wet type process.

12. The method as recited in claim 11, wherein the dry etching has an etch selectivity ratio of the polysilicon layer with respect to the storage node oxide layer of about 40 to about 1.

13. The method as recited in claim 11, wherein the wet etching process uses one of a chemical solution mixed with NH_4OH at a mixing ratio ranges which from about 10 to about 1 and H_2O at a mixing ratio which ranges from about 1 to about 500 and a chemical solution mixed with HF at a mixing ratio which ranges from about 20 to about 1 and HNO_3 having a mixing

ratio which ranges from about 1 to about 100.

14. The method as recited in claim 13, wherein the chemical solution is put into a dipping bath at a temperature maintained in a range from about 4 °C to about 100 °C for about 5 seconds to about 3600 seconds.

15. The method as recited in claim 11, wherein at the step of forming the supporting hole, the polysilicon plug has a target thickness ranging from about 50 Å to about 5000 Å.

16. A capacitor for use in a semiconductor device, comprising:

a substrate;

an inter-layer insulating layer having a contact hole exposing a partial portion of the substrate and being formed on the substrate;

a storage node contact providing a supporting hole at an upper region of the contact hole and filling a partial portion of the contact hole; and

a storage node being connected to the storage node contact wherein a bottom portion of the storage node is filled and secured into the supporting hole.

17. The capacitor as recited in claim 16, further comprising a supporting layer formed on the inter-layer insulating layer and providing a step-like opening in addition

to the supporting hole.

18. The capacitor as recited in claim 17, wherein the supporting layer is a nitride layer.

19. The capacitor as recited in claim 16, wherein the supporting hole has a depth of about 50 Å to about 5000 Å.

20. The capacitor as recited in claim 16, wherein the storage node contact is a polysilicon plug.

21. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a storage node contact connected to the substrate by passing through the inter-layer insulating layer;

forming a multi-layered insulation supporting element on the inter-layer insulating layer, the multi-layered insulation supporting element exposing the storage node contact and including at least one layer providing an under-cut region; and

forming a cylindrical storage node electrically connected to the storage node contact as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element.

22. The method as recited in claim 21, wherein the step

of forming the multi-layered insulation supporting element includes further the steps of:

forming a first etch barrier layer on the inter-layer insulating layer;

forming an insulation layer on the first etch barrier layer;

forming a second etch barrier layer on the insulation layer;

forming an under-cut region in between the first and the second etch barrier layers by selectively removing the insulation layer.

23. The method as recited in claim 22, wherein the step of selectively removing the inter-layer insulating layer employs a wet type dip-out process.

24. The method as recited in claim 22, wherein the insulation layer is an oxide layer formed through a chemical vapor deposition technique, and the first and the second etch barrier layers are nitride layers.

25. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a storage node contact connected to the substrate by passing through the inter-layer insulating layer;

forming a storage node supporting layer on the inter-

layer insulating layer such that an insulation layer is inserted into a space between a first etch barrier layer and a second etch barrier layer;

forming a storage node insulating layer on the storage node supporting layer;

forming a storage node hole by etching the storage node insulating layer and the storage node supporting layer to make an etching process stop at the first etch barrier layer;

removing selectively the storage node insulating layer and the storage node supporting layer to widen a width of the storage node hole and simultaneously form an under-cut region in between the second etch barrier layer and the first etch barrier layer;

forming a cylindrical storage node connected to the storage node contact as a bottom region of the storage node formed in the storage node hole is inserted into the under-cut region; and

removing selectively the storage node insulating layer.

26. The method as recited in claim 25, wherein, at the step of widening the width of the storage node hole and forming the under-cut region in between the second etch barrier layer and the first etch barrier layer, the storage node insulating layer and the storage node supporting layer are selectively etched through a dip process using a wet chemical.

27. The method as recited in claim 26, wherein the storage node insulating layer and the storage node supporting layer are oxide layers, and the first and the second etch barrier layers are nitride layers.

28. The method as recited in claim 26, wherein the dip process uses one of diluted HF, a chemical mixed with HF-based family and a chemical mixed with ammonia-based family at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 1800 seconds.

29. The method as recited in claim 25, wherein the step of removing selectively the storage node insulating layer is carried out at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 3600 seconds with use of a HF-based chemical.

30. The method as recited in claim 25, wherein the step of forming the storage node hole is carried out by employing a dry etching process.